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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
ERIC J STRANG	: EXAMINER: SAXENA, A.
SERIAL NO: 10/673,467	:
FILED: SEPTEMBER 30, 2003	: GROUP ART UNIT: 2128
FOR: SYSTEM AND METHOD FOR USING FIRST-PRINCIPLES SIMULATION TO CONTROL A SEMICONDUCTOR MANUFACTURING PROCESS	:

REPLY BRIEF UNDER 37 CFR 41.41

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is a Reply Brief to the Examiner's Answer dated November 14, 2008.

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I. Status of Claims

Claims 1-54 and 58-60 are pending and appealed. Claims 55-57 and 61 have been cancelled.

Claims 1-21, 23, 25-48, 50, 52-54, and 58-60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Chen (U.S. Pat. No. 5,719,796) and in view of Jain et al ("Mathematical Physical Engine"). Claims 22 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Chen and Jain further in view of Yunemura et al (IEEE Article, "Heat Analysis on Insulated Metal Substrates"). Claims 24 and 51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Chen and Jain further in view of Nikoonahad (U.S. Pat. No. 6,812,045).

II. Grounds of Rejection for Review

Whether the rejection of Claims 1-21, 23, 25-48, 50, 52-54, and 58-60 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Chen (U.S. Pat. No. 5,719,796) and in view of Jain et al ("Mathematical Physical Engine") should be reversed. Whether the rejection of Claims 22 and 49 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Chen and Jain further in view of Yunemura et al (IEEE Article, "Heat Analysis on Insulated Metal Substrates") should be reversed. Whether the rejection of Claims 24 and 51 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Chen and Jain further in view of Nikoonahad (U.S. Pat. No. 6,812,045) should be reversed.

III. Arguments

Claim 1 defines a method of controlling a process performed by a semiconductor processing tool, including:

> 1) inputting process data relating to an actual process being performed by the semiconductor processing tool,
>
> 2) inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool,
>
> 3) performing first principles simulation for the actual process being performed ***during performance of the actual process*** using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, ***said first principles simulation result being produced in a time frame shorter in time than the actual process being performed,***
>
> 4) using the first principles simulation result obtained during performance of the actual process to build an empirical model; and
>
> 5) selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool.

The claim defines clearly a process where data input from an actual process being performed is used for producing a first principles simulation result, produced for the actual process being performed during performance of the actual process. The result obtained is produced in a time frame shorter in time than the actual process being performed. The result obtained is then used to build an empirical model.

The Examiner and the Appellant continue to disagree as to whether Sonderman et al teach performing a first principles simulation for an actual process being performed to provide a first principles simulation result in order to simulate the actual process being performed.

In particular, the Examiner appears to be extensively relying on Figure 1 of Sonderman et al (which is reproduced below).

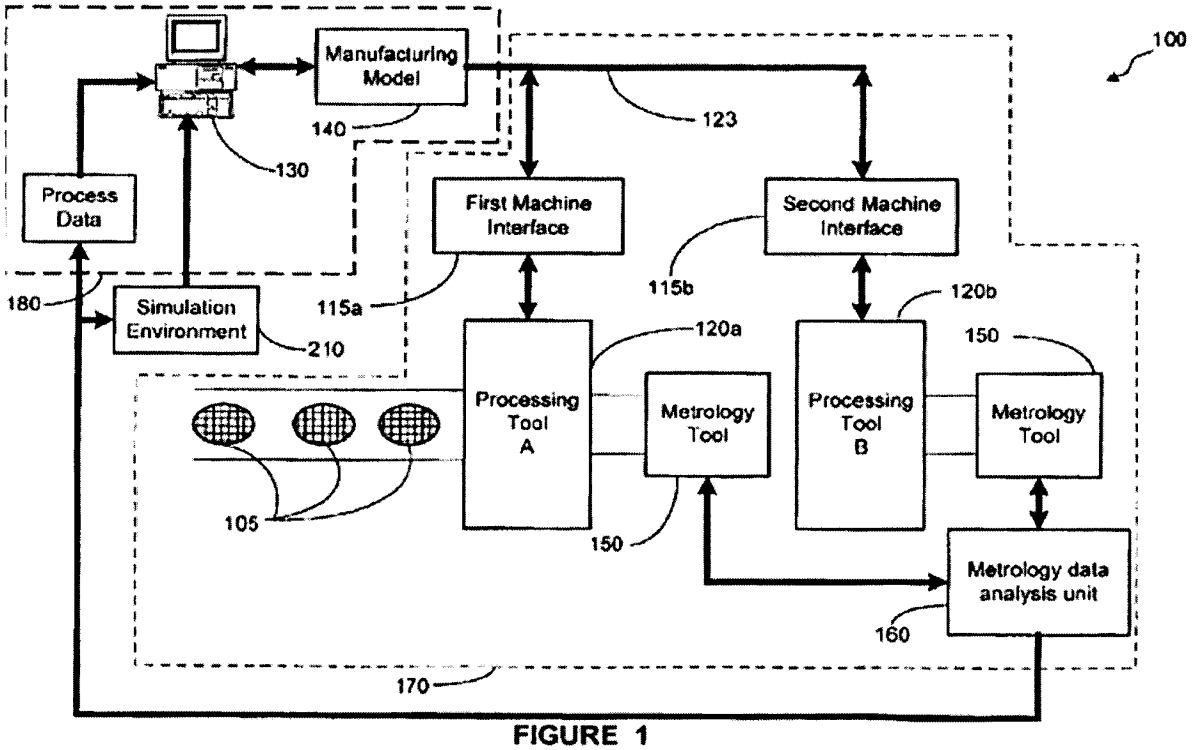

FIGURE 1

The Examiner characterized Sonderman et al by stating on page 24 of the Examiner's Answer that:

> Here examiner would like to emphasize that new control inputs X_{Ti} are generated to control the "subsequent [part of the] process" (applicable to same processes as inputs are pertinent to same process only - e.g. metal deposition on substrate where inputs may specify to deposit more metal) on the silicon wafer S_i.
>
> Arguendo, if Sonderman was intending to use the inputs for the next wafer, he would have stated for silicon wafer S_{i+1}, with emphasis on i+1. Therefore as the limitation "**for the actual process being performed during performance of the actual process,**" is performed during the processing of silicon wafer. (See Sonderman Fig. 1). [Reproduced with emphasis added by the Examiner]

Appellant would like to point out that the Examiner's characterization of Sonderman et al given above does not accurately depict what Sonderman et al actually disclose. Firstly, Sonderman et al disclose "a subsequent process" not "the subsequent part of the process" as the Examiner has stated. The Examiner's characterization of Sonderman et al has a significantly different meaning than the plain words in Sonderman et al. Secondly, the parenthetical statements in the Examiner's characterization are mere speculation, and do not represent disclosures in Sonderman et al.

Furthermore, the Examiner inresponse to Appellant's prior arguments that the simulation results in Sonderman et al are based on historical data characterized Sonderman et al by stating on pages 25 and 26 of the Examiner's Answer that:

> As clearly seen, the control parameter from the process control environment are first feed into the simulation environment, and then the post simulation output, having modified control parameters, is used to control the process control environment. Thus, the results are not based on the historical data for another run, but are from the same run, where the input from the process control environment provided to simulation tool is used to generate modified control parameter for the process control environment. [Reproduced with emphasis added by the Examiner]

Appellant respectfully points out that, at col. 4, line 48, to col. 5, line 10, Sonderman et al specifically states:

> Referring now to FIGS. 1 and 2 simultaneously, one embodiment of an interaction between a process control environment 180, a manufacturing/processing environment 170, and a simulation environment 210 is illustrated. In one embodiment the process control environment 180 receives input data from the simulation environment 210, which is then used to control the operation of the manufacturing environment 170. The integration of the simulation environment 210 and the process control environment 180 into the manufacturing environment 170 facilitates more accurate control of the processing of semiconductor wafers. The simulation environment 210 allows for testing various manufacturing factors in order to study and evaluate the interaction between the manufacturing factors. This evaluation can be used by the system 100 to prompt the process control environment 180 to invoke more accurate process control.

> Furthermore, the simulation environment 210 can be used for f***eedback modification*** of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 ***can send metrology data results*** into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A ***feedback loop*** in then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Appellants point out that there is **no** disclosure here of the claimed performing a first principles simulation ***for the actual process being performed*** to provide a first principles simulation result in order to simulate ***the actual process being performed***.

Reiterating in part, Claim 1 defines:

> inputting process data relating to an actual process being performed by the semiconductor processing tool;
>
> . . . .
>
> performing a first principles simulation for the actual process being performed to provide a first principles simulation result in order to simulate the actual process being performed.

Thus, for Sonderman et al to meet these claim elements, Sonderman et al would have to show input data from the actual process being performed being directly used by the computer system 130 to compute a simulation result for the actual process being performed. Yet, Figure 1 of Sonderman et al shows that the only input to the computer system 130 is by way of metrology data.

Metrology data is data taken on samples after a process has been performed. See Appellant's specification numbered paragraph [0106] for a listing of metrology data taken on a sample from "a process ***performed*** by semiconducting processing tool 102." (emphasis added) Indeed, the second part of the noted above quote from Sonderman et al, states with regard to metrology data and feedback control that:

> The simulation environment 210 can then use ***the metrology data results*** and perform various tests and calculations to provide more accurate, ***modified control parameters*** to the process control environment 180. A ***feedback loop*** in then completed when the process control environment 180 sends the ***modified or adjusted process control parameters*** to the manufacturing environment 170 ***for further processing*** of semiconductor wafers.

If Sondermann et al were able to obtain metrology data on the actual process being performed, Sondermann et al would not have to restrict the use of metrology data to feedback control, but rather could use the metrology data for feedforward control.

More significantly, Appellant's position on this matter is corroborated by col. 4, lines 31-47, of Sonderman et al which specifically states:

> One or more of the semiconductor wafers 105 ***that are processed*** by the processing tools 120a, 120b can also be sent to a metrology tool 150 for acquisition of metrology data. The metrology tool 150 can be a scatterometry data acquisition tool, an overlay-error measurement tool, a critical dimension measurement tool, and the like. In one embodiment, ***one or more processed semiconductor wafers are examined*** by the metrology tool 150. Data from the metrology tool 150 is collected by a metrology data analyzer unit 160. The metrology data analyzer unit 160 organizes, analyses, and correlates scatterometry metrology data acquired by the metrology tool 150, to particular semiconductor wafers 105 that were examined. The metrology data analyzer unit 160 can be a software unit, a hardware unit, or a firmware unit. In one embodiment, the metrology data analyzer unit 160 is integrated into the computer system 130.

Appellant's position on this matter is also corroborated by col. 9, lines 46-51, of Sonderman et al which specifically states:

> The system 100 ***then*** optimizes the simulation (described above) to find more optimal process target (T_i) for each silicon wafer, ***S_i to be processed***. These target values are then used ***t***o generate ***new control inputs, X_{Ti},*** on the line 805 to control ***a subsequent process of a silicon wafer S_i***. [Emphasis added]

The plain reading of this section of Sonderman et al is that the system 100 ***then*** (e.g., at time T1) optimizes the simulation for each silicon wafer, ***S_i to be processed*** (e.g., later at time T2).

In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer ***to be processed***.

Thus, Appellant respectfully submits that Sonderman et al teach performing a simulation result for a process to be performed ***before*** performance of the actual process, and do **not** teach the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.[1]

Other sections of Sonderman et al support Appellant's position on this matter that the simulation results in Sonderman et al are made prior to controlling a subsequent process. For instance, Figure 4 of Sonderman et al (reproduced below) shows that the simulation results are produced ***ahead of performing a process*** and thus are based on historical data.

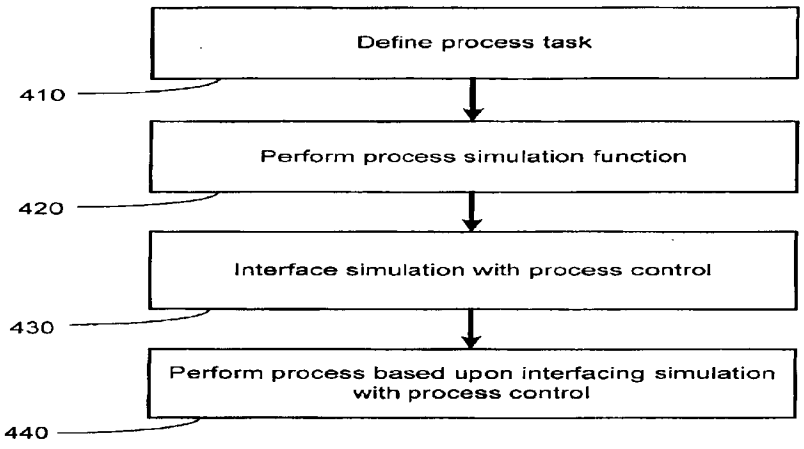

FIGURE 4

With reference to Figure 4, Sonderman et al disclose at col. 6, lines 24-47:

> Turning now to FIG. 4, a flow chart representation of the methods in accordance with the present invention is illustrated. In one embodiment, ***the***

[1] Appellant also points out that Sonderman et al do not disclose or suggest a first principles simulation.

> ***system 100 defines a process task that is to be performed (block 410).*** The process task may be a photolithography process, an etching process, and the like. ***The system 100 then performs a process simulation function*** (block 420). A more detailed description of the process simulation function described in block 420, is illustrated below. In one embodiment, a simulation data set results from the execution of the process simulation function.
>
> ***Once the system 100 performs the process simulation function, the system 100 performs an interfacing function***, which facilitates interfacing of the simulation data with the process control environment 180 (block 430). The process control environment 180 can utilize the simulation data in order to modify or define manufacturing control parameters that control the actual processing steps performed by the system 100. ***Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 <u>then</u> performs a manufacturing process*** based upon the manufacturing parameters defined by the process control environment 180 (block 440). [Emphasis added]

Hence, the process flow in <u>Sonderman et al</u> is straightforward:

1) define a process to be modeled,

2) model the simulation result,

3) interface simulation result to processor, and then

4) run the process under control based on the pre-existing simulation result.

Accordingly, Appellant respectfully submits that <u>Sonderman et al</u> do not disclose and indeed ***teach away*** from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, which is produced for the actual process being performed during performance of the actual process in a time frame shorter in time than the actual process being performed.

The deficiencies in <u>Sonderman et al</u> for teaching 1) performing first principles simulation for the actual process being performed ***during performance of the actual process*** using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, and 2 that the ***first principles simulation result being produced in***

a time frame shorter in time than the actual process being performed are not overcome by Jain et al or Chen.

The Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Jain et al for their teaching of computer encoded differential equations in a mathematical physical engine (MPE) which can be applied to wafer processing. See Office Action, page 13. Jain et al describe at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations.
>
> Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

Thus, as emphasized above, the proposed development work in Jain requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.

The Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Chen for their teaching of creating an empirical model as a statistical model built based on run-to-run or batch-to-batch results and using the result to control the process performed by the semiconductor processing tool as well as the next simulation step See Office Action, page 5. Chen describes col. 3, lines 12-47, and col. 6, lines 34-67, a statistical model. More importantly, Chen describes at cols. 1 and 2 the technical difficulties of conventional manufacturing simulation tools, which prompt Chen to use a statistical simulation, rather than a process simulation based on a mathematical model:

> Process simulation is the usage of processing experiments, typically using a computer, as directed by mathematical models created to describe a process phenomena. Many simulation and analysis tools (for example, Pisces, Medici, Suprem3, Suprem4 and PdFab) have been developed to assist process integration and device development. These tools have not been as widely employed for integrated circuit manufacturing. Generally, these tools are developed primarily for research and development purposes and do not adequately address various difficulties that arise in the manufacturing environment.
>
> * * * *
>
> Manufacturing simulation tools are calibrated prior to performing a simulation test. Calibration is typically accomplished by entering calibrated input parameters that are generated either experimentally or by previous simulation. In conventional manufacturing process calibration, a specified value of a parameter is fitted to produce a specified process output value. Realistic simulation results are rarely achieved using conventional simulation and calibration techniques since these techniques do not capture the true nature and complexity of the manufacturing process. Furthermore, conventional calibration processes require an intense study of device engineers before a simulation tool becomes useful. Thus, the calibration processes cause significant delay in process qualification and improvement. This problem is worsened by the fact that calibration procedures are repeated continuously as the environment in the manufacturing area changes over time.

Chen states at col. 3, lines 13-23:

> In accordance with the present invention, a statistical simulation of a semiconductor fabrication process is performed in parallel with the actual

process. Input parameters extracted from actual fabrication data and expressed in the form of a probability density function are applied to the simulator which, in turn, simulates an actual fabrication process which is modeled as a probability density function. Each simulation step is repeated with a random seed value using a Monte Carlo technique, a trial-and-error method using repeated calculations to determine a best solution to a problem. The simulator generates an output in the form of a probability distribution.

Appellant's position of the deficiencies of Sonderman et al and Jain et al and Chen is corroborated by statements in Appellant's specification. Reproduced below are numbered paragraphs [004] and [005] from the specification:

> These industry and manufacturing challenges have led to interest in more use of computer based modeling and simulation in the semiconductor manufacturing industry. Computer-based modeling and simulation are increasingly being used for prediction of tool performance during the semiconductor manufacturing tool design process. The use of modeling allows the reduction of both cost and time involved in the tool development cycle. Modeling in many disciplines, such as stress, thermal, magnetics, etc., has reached a level of maturity where it can be trusted to provide accurate answers to design questions. Moreover, computer power has been increasing rapidly along with the development of new solution algorithms, both of which resulted in reduction of time required to obtain a simulation result. ***Indeed, the present inventors have recognized that a large number of simulations typically done in the tool design stage can presently be run in times comparable to wafer or wafer cassette processing times.*** These trends have led to the suggestion that simulation capability typically used only for tool design can be implemented directly on the tool itself to aid in various processes performed by the tool. For example, the 2001 International Technology Roadmap for Semiconductors identifies issues impeding the development of on-tool integrated simulation capability as an enabling technology for manufacturing very small features in future semiconductor devices.
>
> ***Indeed, the failure of industry to implement on-tool simulation to facilitate tool processes is primarily due to the need for computational resources capable of performing the simulations in a reasonable time.*** Specifically, the processor capabilities currently dedicated to semiconductor manufacturing tools are typically limited to diagnostic and control functions, and therefore could only perform relatively simple simulations. Thus, the semiconductor manufacturing industry has perceived a need to provide powerful dedicated computers in order to realize meaningful on-tool simulation capabilities. However, dedication of such a computer to the semiconductor processing tool results in wasted computational resources when

> the tool runs processes that use simple simulations, or no simulations at all. This inefficient use of an expensive computational resource has been a major impediment to implementation of simulation capabilities on semiconductor processing tools.

Thus, this part of the specification specifies that the "present inventors" ***not prior work by others*** have recognized that a large number of simulations typically done in the tool ***design stage*** can presently be run in times comparable to wafer or wafer cassette processing times. Moreover, this description does not indicate that a first principles simulation result could be produced in a time frame shorter in time than the actual process being performed, as claimed.

Moreover, the "failure of industry" noted in Appellant's specification emphasized above is evidenced by Kee et al of record.

Kee et al deal with the process control of a Rapid Thermal Processing (RTP) tool and do **not** use real time modeling. RTP tools are tools used in semiconductor manufacturing. Kee et al in detail disclose that:

> The modeling apparatus 101 of the instant invention may also be used to perform an inverse analysis to establish the boundary conditions or parameter values required to achieve a certain function of the thermal system. This allows the apparatus to be used to establish the appropriate process parameters and boundary conditions for the thermal system modeled. In accordance with the instant invention, the inverse analysis can be directly carried out by the modeling apparatus ***rather than using the conventional approach, which merely solves the direct problem repeatedly, in a lengthy and costly iterative process***, to determine appropriate input parameters to achieve a desired result. In other words, in accordance with the instant invention, ***once a particular thermal process is modeled for a particular set of control parameters***, the device may then be used to automatically obtain the necessary control parameters to achieve a desired result by providing the modeling apparatus with parameters corresponding to the desired result.
>
> To carry out the inverse analysis, the modeling apparatus 101 includes an inverse parameter input section 104 also connected to input device 103. A user inputs into the modeling apparatus 101 parameters corresponding to desired results, e.g., desired temperature characteristics of the system, which

> are stored in memory 108. The processing unit 110, under control of modeling program 111, ***uses the previously generated model*** of the thermal system and the parameters held in memory 108 and derives or predicts particular control parameters to meet the constraints entered through the inverse parameter input section 104. This process is more fully described below in connection with the examples provided.[2] [Emphasis added.]

Hence, Kee et al explicitly disclose that a ***previously generated*** model of the thermal system is used to design and control the thermal system. Kee et al exemplify the difficulties of a "conventional approach" which solves spectral radiation transport equations through "a lengthy and costly iterative process." These problems forced Kee et al to use ***pre-generated model results*** for control of a RTP process.

Hence, Kee et al. further Appellant's position on non-obviousness by illustrating the ***technological difficulty*** and ***failure of others*** in producing a first principle simulation result in a time frame shorter in time than the actual process being performed.

Recently published guidelines for the Patent and Trademark Office, published in Federal Register Vol. 72, No. 195, on Wednesday October 10, 2007 entitled: "Examination Guidelines for Determining Obviousness under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International v. Teleflex Inc," indicate that:

> Office personnel should consider all rebuttal evidence that is timely presented by the Applicants when reevaluating any obviousness determination. Rebuttal evidence may include evidence of "secondary considerations," such as "commercial success, long felt but unsolved needs, [and] ***failure of others***", and may also include evidence of unexpected results. Office personnel must articulate findings of fact that support the rationale relied upon in an obviousness rejection. As a result, Applicants are likely to submit evidence to rebut the fact finding made by Office personnel. For example, in the case of a claim to a combination, Applicants may submit evidence or argument to demonstrate that:
>
> (1) one of ordinary skill in the art could not have combined the claimed elements by known methods (e.g., ***due to technological difficulties***);
>
> (2) the elements in combination do not merely perform the function that each element performs separately; or

[2] Kee et al, col. 4, lines 21-50.

(3) the results of the claimed combination were ***unexpected***.

> Once the Applicant has presented rebuttal evidence, Office personnel should reconsider any initial obviousness determination in view of the entire record. All the rejections of record and proposed rejections and their bases should be reviewed to confirm the continued viability. The Office action should clearly communicate the Office's findings and conclusions, articulating how the conclusions are supported by the findings. [Emphasis Added.]

M.P.E.P. § 2143.01(II) indicates that all teachings in the prior art must be considered. M.P.E.P. 2141.03 indicates that the examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time of the invention. Hence, for all these legal considerations, Appellant's description in the specification of the failure of industry to provide computational resources capable of performing the simulations in a reasonable time, and the failure of Kee et al and Chen to produce a first principles simulation result in a time frame shorter in time than the actual process being performed are **all** presented here as rebuttal evidence showing the non-obviousness of the claims.

For all these reasons, Appellant submits that Claims 1, 28 and 58 patentably define over Sonderman et al, Chen, and Jain et al.

Hence, the 35 U.S.C. § 103(a) rejection of Claims 1-21, 23, 25-48, 50, 52-54, and 58 as being unpatentable over Sonderman et al in view of Chen and in view of Jain et al should be reversed.

Regarding Claims 22 and 49, the Office Action applies Yunemura et al to overcome the deficiencies of Sonderman et al and Jain et al regarding the features of Claims 22 and 49 directed to an ANSYS computer code. The Examiner's Answer on page 12 states:

> It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time of the invention was made to apply the teachings of Yunemura and Sonderman and Jain to create an equipment model as disclosed by Sondermann. The motivation to combiner would have been that Yunemura

> teaches heat modeling on a silicon chip affecting thermal conductivity (Yunemra: Pg, 1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure.

Yet, the claimed ANSYS computer code is utilized to perform the first principles simulation on the actual process being performed, as defined in Claim 1 from which Claim 22 depends. Meanwhile, Yunemura et al describe simulation modeling on a silicon chip. Thus, Yunemura et al is directed to heat generation and dissipation of heat from an operating silicon chip, not the simulation of an actual process being used for the manufacturing of a silicon chip.

Thus, the ANSYS computer codes in Yunemura et al are **not** directed to modeling of a processing condition. Accordingly, a combination of Yunemura et al and Sonderman and Jain would not produce an ANSYS computer code utilized to perform the first principles simulation on the actual process being performed. Thus, the asserted combination fails to meet the elements of dependent Claims 22 and 49. Moreover, given the differences between the modeling of heat dissipation in an actual device chip and a method of controlling a process performed by a semiconductor processing tool, one of ordinary skill in the art would have no rationale to consider or to use Yunemura et al for developing an ANSYS computer code for controlling a process performed by a semiconductor processing tool.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 22 and 49 as being unpatentable over Sonderman et al, Chen, Jain et al, and Yunemura et al should be reversed.

Regarding Claims 24 and 51, the Office Action applied Nikoonahad to overcome the deficiencies of Sonderman et al, Chen, and Jain et al regarding the features of Claims 24 and 51. Claim 24 defines:

> 24. The method of Claim 23, wherein said using the first principles simulation result to control comprises:
> controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

Yet, the examiner's position as to why it would have been obvious to combine Nikoonahad to Sonderman et al, Chen, and Jain et al is merely a statement of the teachings being analogous art and both concerning modeling.

Yet, KSR requires an articulated rationale as to why the claimed features are obvious and indicates that conclusory statements are not sufficient. Indeed, the Guidelines for the Patent and Trademark Office, published in Federal Register Vol. 72, No. 195, entitled: "Examination Guidelines for Determining Obviousness under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International v. Teleflex Inc," indicate that:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Court quoting In re Kahn 41 stated that " '[R]ejections on obviousness ***cannot be sustained by mere conclusory statements***; instead, there ***must be some articulated reasoning with some rational underpinning*** to support the legal conclusion of obviousness.'''

M.P.E.P. § 2141.03 as revised adopts the Federal Register Guidelines.

Moreover, Figure 10 of Nikoonahad relates to the mathematical simulation of optical data taken from a sample after a process has been performed, where the simulation is used to determine from the optical data features of the processed sample such as for example the height, critical distance (CD), and taper, as shown in Figure 8 reproduced below:

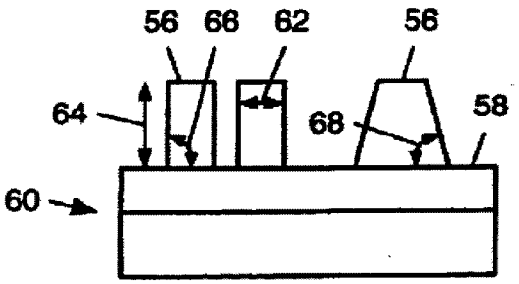

Fig. 8

Furthermore, Figure 13 of Nikoonahad (reproduced below) shows that the optical measurement system 32 is located either besides a lithography tool 130 or interface system 152 with robotic transfers 136 for the transfer of a sample from processing chambers 132, 144, 146, 148, 150, 154, and 156, to the lithography tool 130 or to the interface system 152.

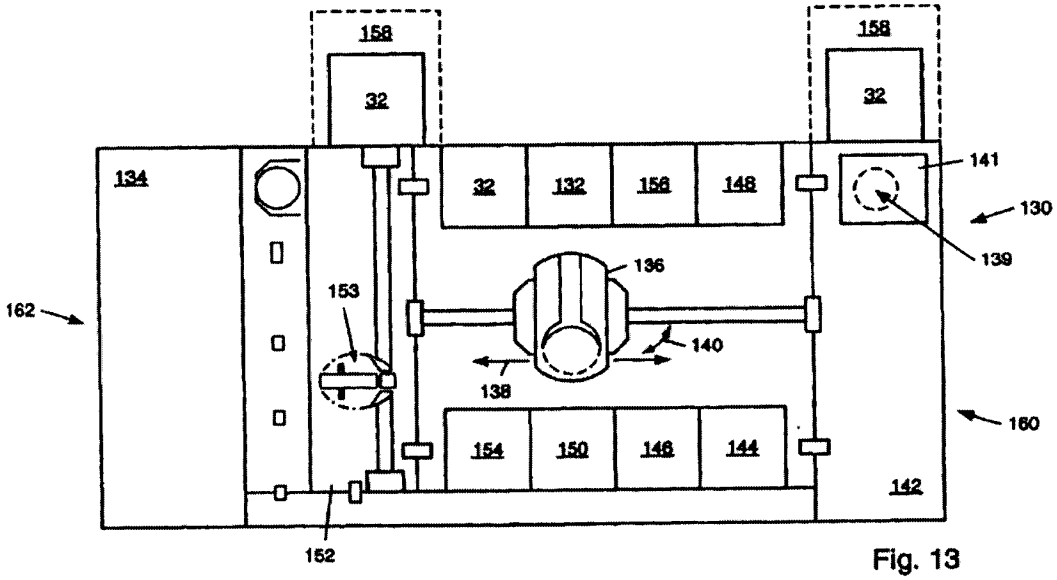

Fig. 13

Thus, the "simulations" in Nikoonahad are post-process simulations used to interpret optical data taken on a processed sample. There is no rationale, suggestion, or motivation that these "simulations" in Nikoonahad have any pertinence or relationship to the claimed

using the first principles simulation result to control at least one of a chemical vapor deposition system and a physical vapor deposition system, as defined for example in Claim 24.

Hence, with there still being no articulated reasons given by the Examiner which would support why it would be obvious to arrive at the elements of Claims 24 and 51, based on Nikoonahad, the rejections of Claims 24 and 51 should be reversed.

III. Conclusion

Appellant request on the basis of the arguments presented above that the outstanding grounds for the rejection be reversed. Appellant submits that the application is in condition for allowance.

Respectfully submitted,

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